personal computing products

CX82310

AccessRunner® Single Chip ADSL Router

Data Sheet (Preliminary)

Doc. No. 101719A
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CONEXANT™

Revision Record

Revision	Date	Comments
A	1/15/2002	Initial release.

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1 Introduction

1.1 Overview

The Conexant™ AccessRunner® CX82310 Single Chip ADSL Router combines an "always-on" high speed Asymmetric Digital Subscriber Line (ADSL) connection to the telephone line, and Ethernet and/or Universal Serial Bus (USB) connection to a host PC or Ethernet hub into a single cost-effective solution.

Conexant's CX82310 ADSL Router is compliant with the full-rate ANSI T1.413 Issue 2 and ITU G.dmt (G.992.1) ADSL standards, and with the splitterless ITU G.lite (G.992.2) specification. Both Annex A (ADSL over POTS) and Annex B (ADSL over ISDN) of G.992.1 and G.992.2 are supported. This rate-adaptive solution is designed for Customer Premise Equipment and supports downstream data rates of up to 8 Mbps and upstream data rates of up to 1 Mbps.

The CX82310 ADSL Router simultaneously supports both USB and Ethernet to enable the widest array of host connectivity. The Router performs ATM Segmentation and Reassembly (SAR), industry standards for PPP over ATM (RFC 2364), bridged/routed Ethernet over ATM (RFC 2864/1483), Classical IP over ATM (RFC 1577), and PPP over Ethernet (RFC 2516), resulting in a cost-effective solution suitable for both full rate and G.lite applications. The non-reliance on host PC software drivers make the Conexant CX82310 Single Chip ADSL Router ideal for ubiquitous broadband connectivity that is not limited by host OS, processor type/speed, or memory.

The USB specification version 1.1 and IEEE 802.3 Ethernet specification are supported for connectivity to a host PC or other USB or Ethernet capable device. Auto-selection of which interface is active, as well as simultaneous operation of the both USB and Ethernet, are supported.

Networking support includes both bridge and router modes. Router Mode supports advanced features such as Network Address Translation (NAT), Dynamic Host Configuration Protocol (DHCP), and Routing Information Protocol (RIPv2).

A high performance, 16-bit wide, parallel expansion bus is available for additional functionality. This expansion bus provides a simple interface to a PCMCIA 802.11b wireless system. Additionally, the expansion bus can be used to interface to a V.92/V.90 backup system. The device can optionally run the stateful packet inspection (SPI)-based eFirewall from Intoto, Inc.

All setup and provisioning is performed by a simple, easy-to-use, Web interface.

The CX82310 ADSL Router integrates the following four hardware functions (see Table 1-1, Figure 1-1, and Figure 1-2):

- Network Processor
- ADSL DMT Engine
- Analog Front End
- Line Driver

Table 1-1. AccessRunner CX82310 ADSL Router Device Set Ordering Information

Order No./Part No.		Supported Functions			
Device Set Order No.	**ADSL Router [17 mm x 17 mm FPBGA] Part No.**	**G.992.1/G.992.2 Annex A**	**G.992.1/G.992.2 Annex B**	**802.11b Interface**	**Intoto Firewall**
DSAR-L20A-519	CX82310-11	Yes	No	No	No
DSAR-L20B-519	CX82310-21	Yes	Yes	No	No
DSAR-L30A-519	CX82310-31	Yes	No	Yes	No
DSAR-L40B-519	CX82310-41	Yes	Yes	Yes	No
DSAR-L50A-519	CX82310-51	Yes	No	No	Yes
DSAR-L60B-519	CX82310-61	Yes	Yes	No	Yes
DSAR-L70A-519	CX82310-71	Yes	No	Yes	Yes
DSAR-L80B-519	CX82310-81	Yes	Yes	Yes	Yes

Figure 1-1. AccessRunner CX82310 ADSL Router Simplified Hardware Interface

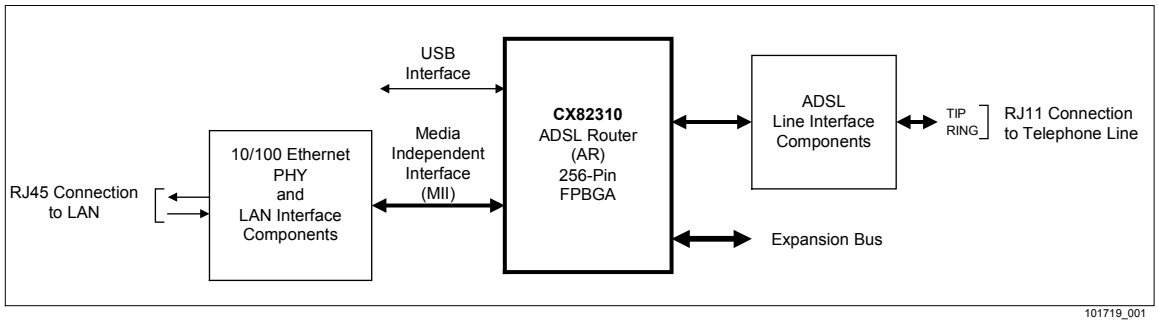
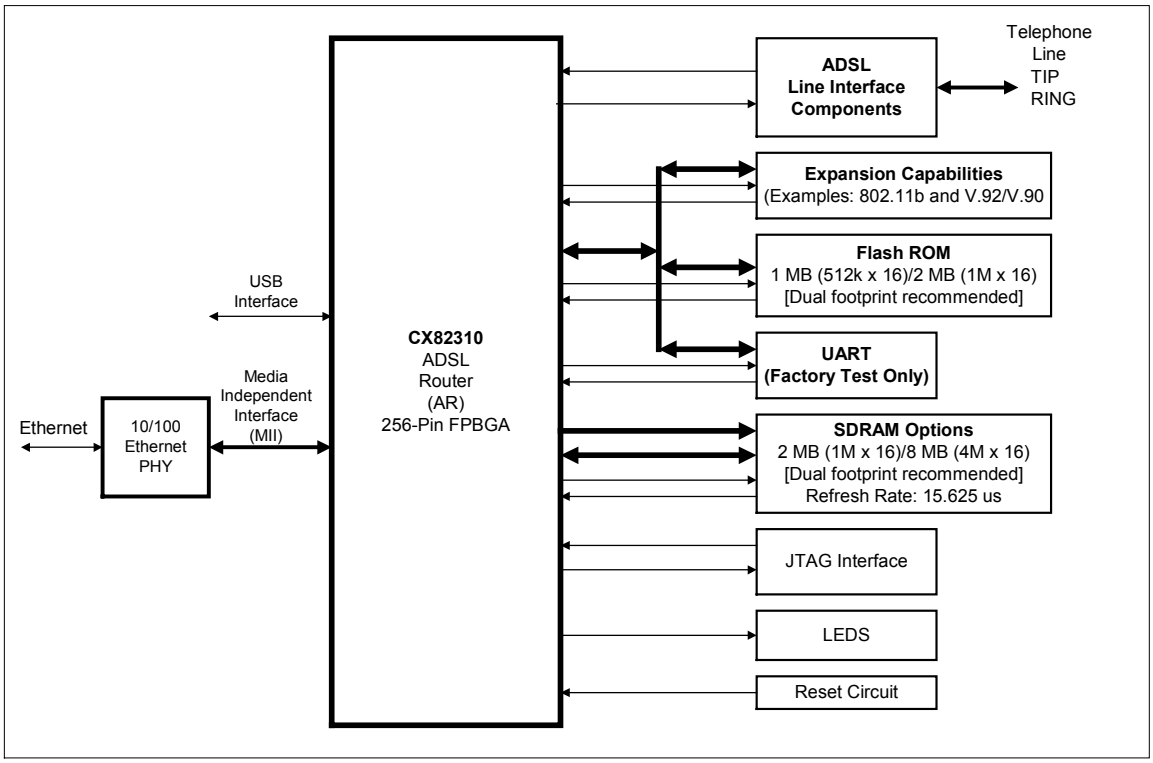


Figure 1-2. AccessRunner CX82310 ADSL Router Device Major Interfaces



The CX82310 ADSL Router is packaged in a 256-pin fine pitch ball grid array (FPBGA).

ADSL is a transmission technology used to carry user data over a single twisted-pair line between the Central Office and the Customer Premises. The downstream (Central Office to Customer Premises) direction typically supports a much higher data rate than the upstream or return (Customer Premises to Central Office) channel. This asymmetric nature lends itself to applications such as Internet access and video delivery. The downstream data rates can go up to 8 Mbps. The upstream data rates can go up to 1 Mbps. Actual data rates depend on the transceiver implementation, loop length, impairments, and transmitted power.

The CX82310 Single Chip ADSL Router device is based upon a scalable architecture. This architecture enables the device set to support splitterless G.lite as well as splittered and splitterless full-rate ADSL. G.lite enables telephone companies to deploy consumer-oriented, “always on” 1.5 Mbps Internet access services without the need for splitter equipment, micro-filters, or wiring changes at the customer premises.

1.2 Applications

- ADSL Customer Premise Equipment
- ADSL – Ethernet bridges
- ADSL – Ethernet routers
- ADSL router for embedded platforms
- ADSL router with V.92 backup
- ADSL – wireless access point
- ADSL – wireless routers

1.3 Features

1.3.1 Protocols/Interfaces

- ADSL Compliance
  - Compliant with ADSL standards
    - Full-rate ANSI T1.413 Issue 2 and ITU G.dmt (G.992.1) standards
    - Splitterless ITU G.lite (G.992.2) specification
    - ADSL over POTS (Annex A) and ADSL over ISDN (Annex B)
  - DMT modulation and demodulation
  - Full-rate adaptive modem
    - Maximum downstream rate of 8 Mbps
    - Maximum upstream rate of 1 Mbps
  - Tone detection for low power mode
  - Supports splitterless ADSL implementation
  - Supports Dying Gasp
- ATM Protocols
  - WAN mode support: PPP over ATM (RFC 2364) and PPP over Ethernet (RFC 2516)
  - LAN mode support: bridged/routed Ethernet over ATM (RFC 1483) and Classical IP over ATM (RFC 1577)
  - ATM Forum UNI 3.1/4.0 PVC
  - Up to 8 VCs (Virtual Circuits)
  - ATM SAR (Segmentation and Reassembly)
  - ATM AAL5 (Adaption Layer type 5)
  - OAM F4/F5
- Bridge Mode
  - Ethernet to ADSL self-learning Transparent Bridging (IEEE 802.1D)
  - Supports up to 128 MAC learning addresses
- Router Mode
  - IP routing–RIPv2 (backward compatible with RIPv1)
  - Static routing
  - DHCP (Dynamic Host Configuration Protocol) Server and Client
  - NAPT (Network Address and Port Translation)
  - NAT (Network Address Translation)
  - ICMP (Internet Control Message Protocol)
  - Simultaneous USB and Ethernet operation
  - IGMP (Internet Group Management Protocol)
- Security
  - User authentication for PPP
  - PAP (Password Authentication Protocol)
  - CHAP (Challenge Authentication Protocol)
  - Password protected system management

- SPI Firewall (optional)
  - eFirewall from Intoto, Inc.
- Ethernet interface
  - Compatible with IEEE 802.3 standard
  - 10/100 Mbps auto selection
- USB host interface
  - USB 1.1 compatible
  - USB full speed (12 Mbps)
  - Vendor specific descriptors
- 802.11b interface (optional)
  - Support for Intersil PRISM-based designs
  - WiFi ready
  - Connects to an 802.11b PCMCIA card
  - 128-bit and 64-bit WEP support
- HTTP Web-based management
  - Firmware upgrade via FTP
  - Customizable Web pages
  - WAN and LAN side connection statistics
  - Configuration of static routes and Routing table
  - Configuration of NAT/NAPT
  - Password protected access
  - Selection of Bridge or Router Mode
  - PPP user ID and password
  - Configuration of VCs (Virtual Circuits)

1.3.2 Hardware Functions

Network Processor

- ARM940T Processor
- 4 kB data cache and 4 kB instruction cache
- 168 MHz operation
- ATM AAL5/UBR/CBR SAR
- USB 1.1 interface
- 10/100 Mbps Ethernet Media Access Controller (MAC)
  - Media Independent Interface (MII)
- External Memory Controller (EMC) supports up to 8 MB SDRAM
- Parallel interface for Flash ROM, optional UART, and expansion capabilities such as 802.11b or V.92/V.90
- JTAG interface
- GPIO

ADSL DMT Engine

- No external Interleave RAM required
- Echo cancellation
- Digital interface and rate buffering
- ADSL framing
- Trellis coding
- Forward Error Correction (FEC) encoding and decoding and interleaving
- Constellation encoding/decoding
- IFFT modulation and FFT demodulation
- Transmit and receive signal digital filtering
- Time domain equalization
- Frequency domain equalization
- Clock recovery
- CRC and scrambling
- Digital interface framing
- ATM mode
- Bit-synchronous mode

Analog Front End

- Receive signal path includes:
  - Integrated hybrid receiver circuit with programmable gain
  - High pass filtering and 27 dB of Automatic Gain Control (AGC) to improve signal-to-echo ratio
  - 14-bit ADC
- Transmit signal path includes:
  - 30 dB of AGC for transmit power control
  - Low pass filtering to suppress noise in the receive band
  - 14-bit DAC
- Independent digital serial data and control interfaces
- Low power tone detection mode

Line Driver

- Differential input and output line driver
- Line impedance matching during power-down
- Fixed differential gain

1.3.3 General

- 256-Pin 17 mm x 17 mm FPBGA
- Signaling level: +3.3 V
- Line driver supply voltage: +5 V
- Supply voltage: +3.3 V

1.4 Reference Design

A reference design for an ADSL Router is available to minimize application design time and costs.

The card is pretested to pass FCC Part 15 and Part 68 for immediate manufacturing.

A design package is available in electronic form. The design package includes files for schematics, bill of materials (BOM), vendor part list (VPL), board layout (Gerber format), and documentation.

The design can also be used for the basis of a custom design by the OEM to accelerate design completion for rapid market entry.

1.5 Reference Documents

Title	Document No.
CX82310 Single Chip ADSL Router Programming Guide	101920

2 System Description

2.1 General Description

The CX82310 ADSL Router solution hardware connects to a host PC or Ethernet hub via USB or Ethernet interface, and, optionally, to a wireless network via an 802.11b PCMCIA card. CX82310 ADSL Router device and embedded system firmware are provided. The OEM adds a crystal circuit, Ethernet PHY, ROM, SDRAM, LEDs, optional 802.11b PCMCIA card, and other components. All firmware to support a full rate and/or G.lite ADSL Router is provided. HTTP web-based control/configuration ability is supported. A Flash ROM programming utility is also provided.

2.1.1 External ROM and Power Up Procedure

The CX82310 ADSL Router boots from external ROM. Upon power up, the Ethernet interface is assumed to be the active interface until a USB cable is plugged in, at which time the USB interface is activated. Simultaneous operation of both USB and Ethernet interface is supported. The external ROM contains default configuration information that is used. This default configuration can be modified by the OEM. If a USB cable is plugged in, the descriptor information is read from the external ROM and the device is enumerated. This descriptor information and other configuration information can be modified by the OEM.

2.1.2 Flash ROM Programming Utility

The OEM-supplied Flash ROM is required to store program firmware, configuration information, and USB descriptor information. A Flash ROM Programming Utility is available for the OEM to use to program ROM with a custom ROM image. In order to run the program utility, the CX82310 must be set to boot from internal memory. For more information about this utility, refer to firmware release notes.

2.1.3 Web-Based Management

User configuration and management is done via an embedded Web Server running on the CX82310 ADSL Router. Configuration can be accomplished when either the USB or Ethernet interface is active. The web interface, including design of HTML pages can be customized by the OEM.

The configuration web server can be used to monitor and control ADSL line and call activity, accumulate ADSL line and call statistics, and identify the software and connection information. There are different levels of information: 1) User and 2) Administrator.

2.1.4 Flash File System

A DOS file system is implemented for the external Flash ROM, making reading from and writing to files in the flash trivial, and thus easily allowing an OEM to load configuration information, HTML pages and USB descriptor information into the flash device.

2.2 ADSL Operation

2.2.1 ADSL Operating Modes

Full Rate ADSL Modes

Both T1.413 and G.992.1 (G.dmt) line coding schemes are supported for downstream rates up to 8 Mbps and upstream rates up to 1 Mbps in 32 kbps increments. User selection of mode is supported through the Web-based management facility, however, auto-provisioning is supported so that the appropriate modulation is automatically selected based on what is supported by the DSL Access Multiplexer (DSLAM) at the Central Office. When operating in one of the full rate modes, the low and high frequency bands must be separated with a filter. This can be done with either a service provider-installed splitter (known as "splittered ADSL"), or with the use of distributed micro-filters in line with each POTS device on the circuit (known as "splitterless full-rate ADSL"). Both deployment models are supported. G.992.1 Annex A and Annex B are supported.

G.lite Splitterless Mode

G.992.2 (G.lite) splitterless mode is supported for downstream rates up to 1.5 Mbps and upstream rates up to 512 kbps in 32 kbps increments. User selection of mode is supported through the Web-based management facility, however, auto-provisioning is supported so that the appropriate modulation is automatically selected based on what is supported by the DSLAM at the Central Office. When operating in splitterless mode, the low and high frequency bands do not need to be separated with a filter, and neither a service provider installed splitter, nor distributed micro-filters are required. G.992.2 Annex A and Annex B are supported.

LAN Encapsulation Modes

RFC-2864/1483 (bridged/routed Ethernet over ATM) and RFC-1577 (Classical IP over ATM) are the supported LAN encapsulation modes. These protocols provide LLC encapsulation for carrying network interconnect traffic over a single ATM AAL5 Virtual Connection. LLC encapsulation is desirable when it is not practical to have a separate VC for each carried protocol, such as with an ATM network that only supports Permanent Virtual Circuits (PVCs). The provided embedded software automatically establishes a "connection-less" call using the defined PVC and encapsulated Ethernet bridged frames.

WAN Encapsulation Modes

RFC-2364 (PPP over ATM) and RFC-2516 (PPP over Ethernet) are the supported WAN encapsulation modes. Point-to-Point Protocol provides a method of transporting multi-protocol packets over point-to-point links. Point-to-point links allow for services such as Link Control Protocol, Network-layer Control Protocol, and authentication. The PPP over

ATM standard brings these point-to-point services to the ATM network where they are not inherently supported.

User selection of encapsulation mode can be done via the Web-based management facility.

2.2.2 Host Software

For Ethernet interface, no host software is required. The ADSL Router can be connected to any interface that supports IEEE 802.3 Ethernet.

A Windows host driver is supplied for USB support on a Windows host PC.

2.2.3 ATM Segmentation and Reassembly (SAR)

The CX82310 ADSL Router performs the ATM Segmentation and Reassembly. The SAR sublayer transmitter segments the higher layer information into a size suitable for the payload of the ATM cells of a virtual connection. The receiver reassembles the contents of the cells of a virtual connection into data units to be delivered to higher layers.

The Convergence Sublayer performs message identification and clock recovery. Additionally, the CS of the AAL converts the user service information coming from the upper layer into a protocol data unit (PDU), and also carry out the opposite process at the receiver.

Unspecified Bit Rate (UBR) service allows a connection to be established without specifying the bandwidth expected from the connection. The network makes no guarantees for UBR service: it establishes the route but does not commit bandwidth. UBR can be used for applications that have no delivery constraints and do their own error and flow control. Examples of potential uses or UBR are e-mail and file transfer, as neither application has real-time characteristics.

Constant Bit Rate (CBR) service allows a connection to be established with a specified expected bandwidth. CBR can be used for an application such as video delivery.

2.2.4 Bridge Mode

Bridge Mode is used when there is one PC connected to the LAN-side Ethernet or USB port. IEEE 802.1D method of transport bridging is used to bridge between the WAN (ADSL) side and the LAN (Ethernet or USB) side, i.e., to store and forward. Bridge Mode can be used with both WAN (PPP over Ethernet) or LAN (bridged/routed Ethernet over ATM) modes. WAN Mode is supported with a PPP over Ethernet Client on the LAN-side PC.

2.2.5 Router Mode

Router Mode is used when there is more than one PC connected to the LAN-side Ethernet and/or USB port. This enables the ADSL WAN access to be shared with multiple nodes on the LAN. Both WAN encapsulations (PPP over ATM or PPP over Ethernet) and LAN encapsulations (bridged/routed Ethernet over ATM or Classical IP over ATM) can be used. Both static IP and RIPv2 are supported. Additionally, Network Address Translation (NAT) is supported so that one WAN-side IP address can be shared among multiple LAN-side devices. DHCP is used to serve each LAN-side device an IP address.

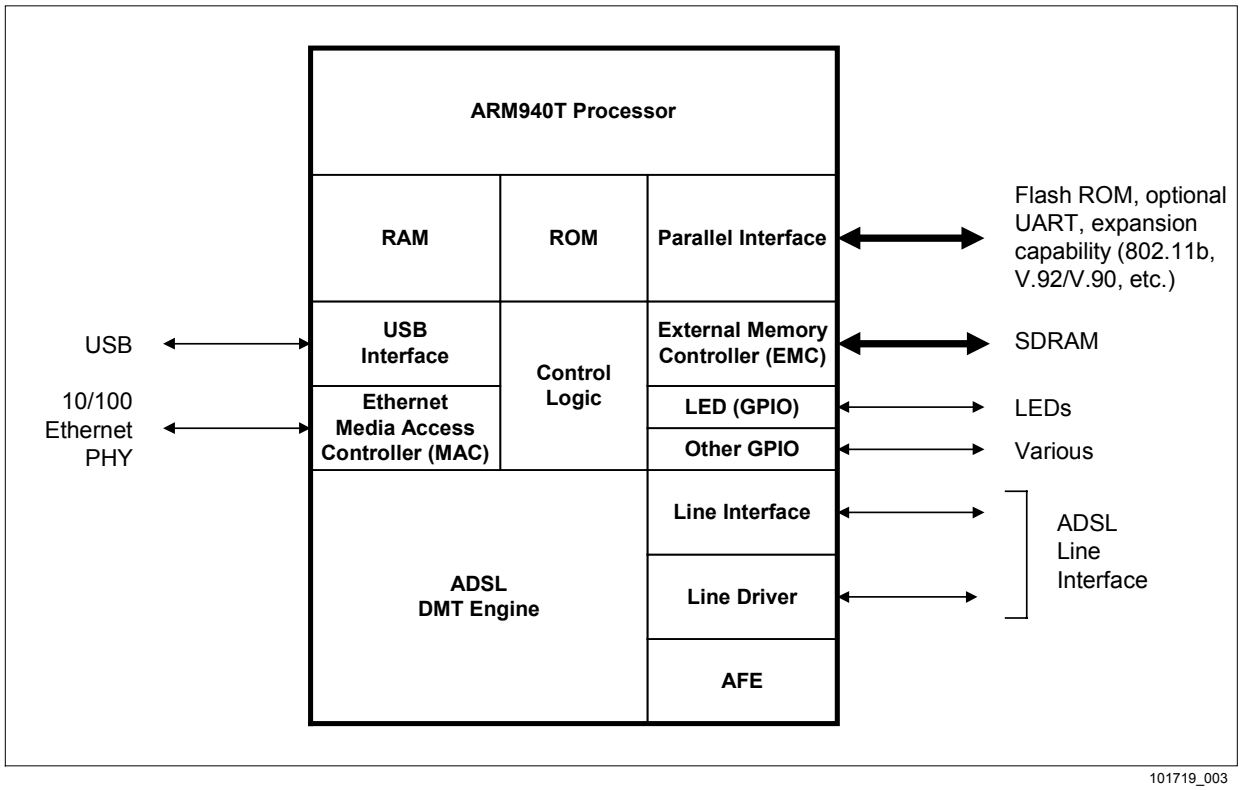
2.3 CX82310 ADSL Router Device Description

The CX82310 ADSL Router is the bridge interface between the ADSL line and the host computer or other Ethernet or USB device. It provides control, interface, and data manipulation for internal ADSL DMT Engine, Analog Front End (AFE), Line Driver (LD), and Line Interface (LI) hardware functions and for external hybrid circuitry. A block diagram of the CX82310 ADSL Router is shown in Figure 2-1.

The CX82310 ADSL Router USB interface is compatible with USB Specification Rev. 1.1 and supports full-speed (12 Mbps) USB device implementation. The CX82310 Router Ethernet interface conforms with the IEEE 802.3 Ethernet standard.

The CX82310 operates from +3.3 V and +5 V supplies. The CX82310 operates with +3.3V interface signals.

Figure 2-1. CX82310 ADSL Router Block Diagram



2.3.1 General Hardware Functions

ARM940T Processor

The ARM940T Processor, running at 168 MHz, provides the controller and supervisory tasks of the ADSL Router system. It also moves data between the USB or Ethernet interface and the ADSL interface. Control code for the ARM is executed from external memory under control of the External Memory Controller (EMC). ATM SAR, encapsulation protocols, all bridge and routing, and Web Server functions are run on the ARM940T Processor.

External Memory Controller

The External Memory Controller (EMC) provides a 16-bit interface to support up to 8 Mbytes of external memory. SDRAM or SRAM is supported to maintain lowest cost of external memory. There can be 1 (16 bits wide) or 2 (8 bits wide) memories that can reside on the EMC bus. This bus is not shared with any other functions so activity on this bus can be concurrent with asynchronous and independent USB/Ethernet and ADSL data transfers.

Parallel Interface

The Parallel Interface is a 16-bit data and 21-bit address bus connecting to the Flash ROM of up to 4Mbytes (256k x 16), optional UART, or other peripheral device, such as 802.11b PCMCIA card, or V.92/V.90 modem.

USB Interface

The USB Interface is responsible for data transfer to and from the USB, by extracting clock and data from the USB cable. It also handles the front end functions of the USB protocol such as Sync Field Identification, NRZI-NRZ Conversion, Bit Stripping and Stuffing, and CRC functions. Additionally, the USB port converts the serial packet to 8-bit parallel data. Control transfers addressed to End Point Zero are handled by the USB port.

Ethernet Media Access Controller

The Router supports the Media Access Controller (MAC) sublayer of IEEE 802.3. It can operate in half-duplex or full-duplex mode. In half-duplex mode, the Router checks the line condition before starting to transmit. If the line is clear, the Router starts transmitting. Full-duplex operation allows simultaneous transmission and reception of data.

The MAC has a Media Independent Interface (MII) that provides a port for transmit and receive data that is media independent, multi-vendor interoperable, and supports all data rates and physical standards. The port consists of data paths that are 4 bits wide in each direction, and includes control and management signals.

General Purpose Input/Output Interface

Most General Purpose Input/Output (GPIO) pins are programmed for dedicated system functions or reserved for test or growth functions and are not available for user assignment. Each GPIO pin is controlled individually for input/output direction. All GPIO pins can serve as external interrupt inputs.

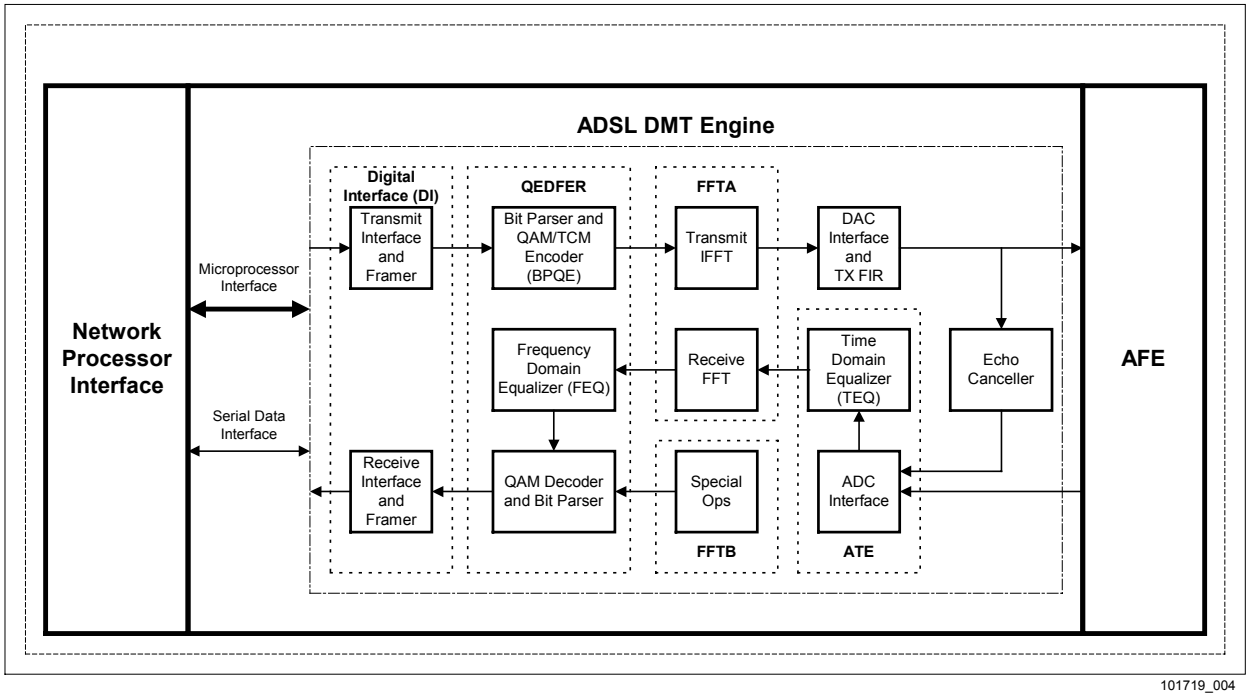
LED Interface

Four GPIO lines are used to support the following LED signals: Ready, Showtime, ADSL TXD, and ADSL RXD.

2.3.2 ADSL DMT Engine

The ADSL DMT Engine is a T1.413 Issue 2, G.992.1, and G.992.2 compliant custom digital signal processing (DSP) hardware element built specifically for DMT ADSL transmission for use in the ADSL Router. Annex A and Annex B are supported. A block diagram of the ADSL DMT Engine is shown in Figure 2-2.

Figure 2-2. ADSL DMT Engine Block Diagram



ATM Transmission Convergence

In the transmit direction, the ATM Transmission Convergence (TC) block embeds ATM cells into the serial data stream being fed into the digital interface, i.e., the CX82310 ADSL Router. In the receive direction, this block extracts the ATM cell boundaries from the serial data stream coming from the digital interface

Digital Interface

The Digital Interface (DI) Transmit Block performs the following functions: transmit data multiplexing and buffering, fast and interleave data stream framing, transmit data synchronization control, eoc/aoc insertion, CRC encoding, scrambling, FEC encoding, and data interleaving.

The DI Receive Block performs the following functions: data de-interleaving, FEC decoding, descrambling, CRC check, receive data synchronization and receive clock generation, demultiplexing and buffering of receive data and receive eoc/aoc.

QAM Encoder/Decoder

The QAM Encoder/Decoder performs the following functions: constellation encoding, clock recovery, receive gain compensation, frequency domain equalization (FEQ), slicing, and constellation decoding. The block also performs other functions such as frequency domain signal processing, signal power, error power averaging and computations related to frequency domain training.

FFT

The FFT performs IFFT for modulation of the transmit symbol, and FFT for demodulation of the receive symbol.

Analog Front End Interface

The Analog Front End (AFE) interface performs the following functions: transmit signal filtering, time domain equalization, and time domain signal power averaging, and echo cancellation (EC).

Microcontroller Interface

The microcontroller interface enables the CX82310 ADSL Router to set parameters to control DSP sequencing and to read/write coefficients or data.

2.3.3 Analog Front End

The Analog Front End (AFE) can support full-rate and G.lite (G.992.2) ADSL Routers. The AFE interfaces with the CX82310 LD Function and the hybrid receive circuitry on the analog side, and with the CX82310 ADSL DMT Engine on the digital side.

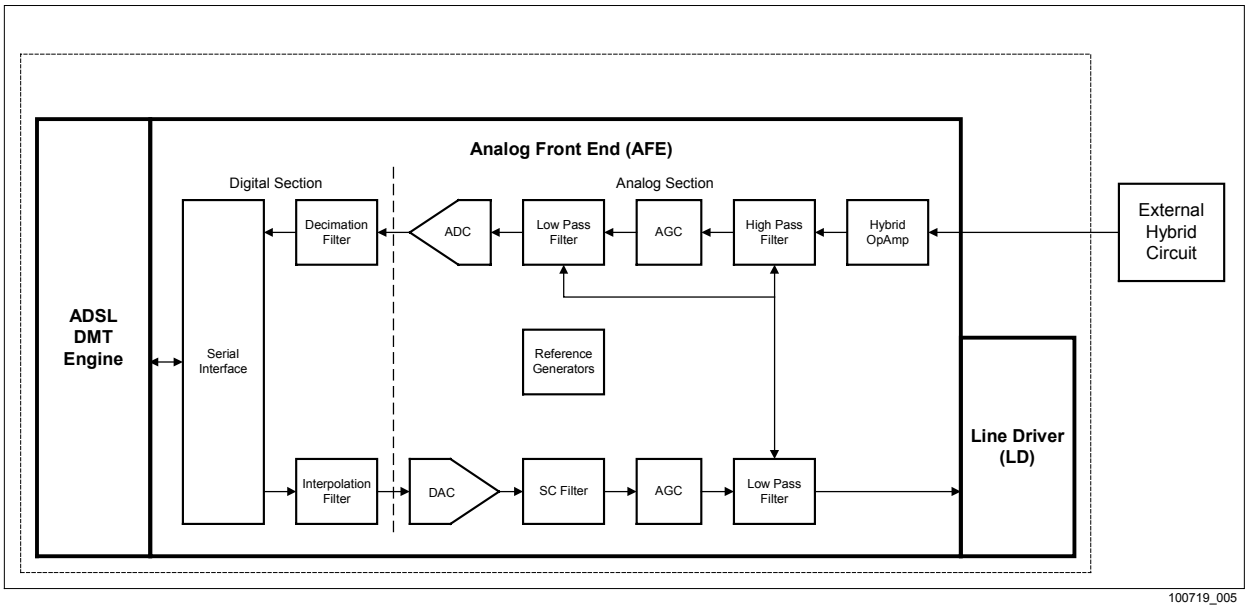
The receive section filters out the unwanted echo and boosts the wanted signal before performing an analog-to-digital (A/D) conversion.

The transmit section converts digital data to analog signals and performs a smoothing operation before presenting the signals to the line driver.

Wakeup in G.lite mode is supported by tone detection circuitry integrated in the AFE.

A block diagram of the CX82310 AFE Function is shown in Figure 2-3.

Figure 2-3. Analog Front End Block Diagram

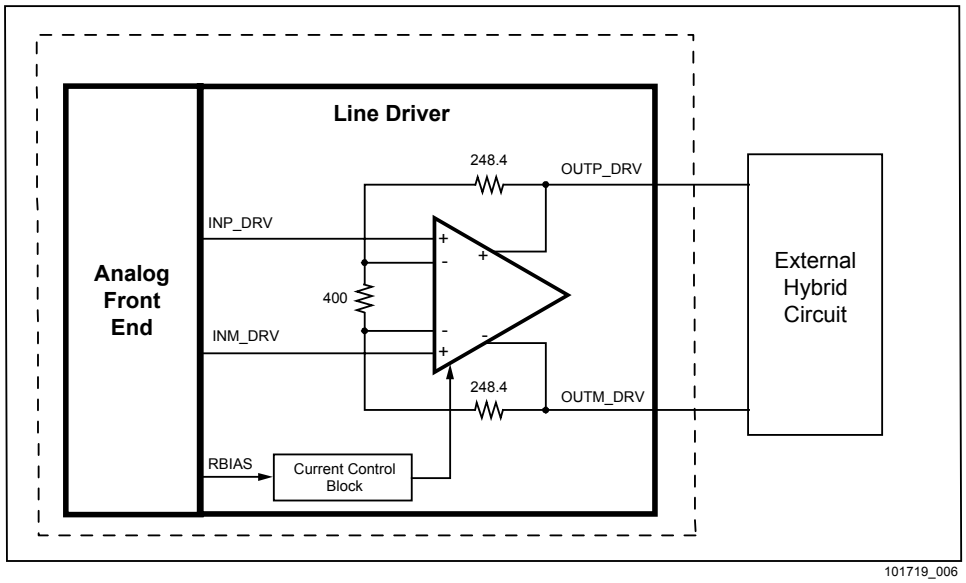


2.3.4 Line Driver

The Line Driver supports full-rate (T1.413 and G.992.1) and G.lite (G.992.2) ADSL Routers. It is optimized for ideal ADSL performance providing low noise, high bandwidth, and superior linearity. The LD transmits a DMT modulated signal in the 25 – 132 kHz band.

Internal load balancing prevents the CX82310 LD Function from loading the system when in a power down state. A block diagram of the LD is shown in Figure 2-4.

Figure 2-4. Line Driver Block Diagram



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3 Hardware Interface

3.1 CX82310 ADSL Router Hardware Interface Signals

This section identifies and describes the CX83210 hardware interface signals for an ADSL router application. Software-assigned GPIO signals are identified by ADSL application signal labels.

The CX82310 can also be connected to an 802.11b interface for Wireless ADSL router applications (see Section 3.2).

3.1.1 CX82310 ADSL Router Signal Interface, Pin Assignments, and Signal Definitions

CX82310 ADSL Router hardware interface signals are shown in Figure 3-1.

CX82310 ADSL Router pin assignments are shown in Figure 3-2 and are listed in Table 3-1.

CX82310 ADSL Router hardware interface signals are defined in Table 3-2.

Figure 3-1. CX82310 ADSL Router Hardware Interface Signals

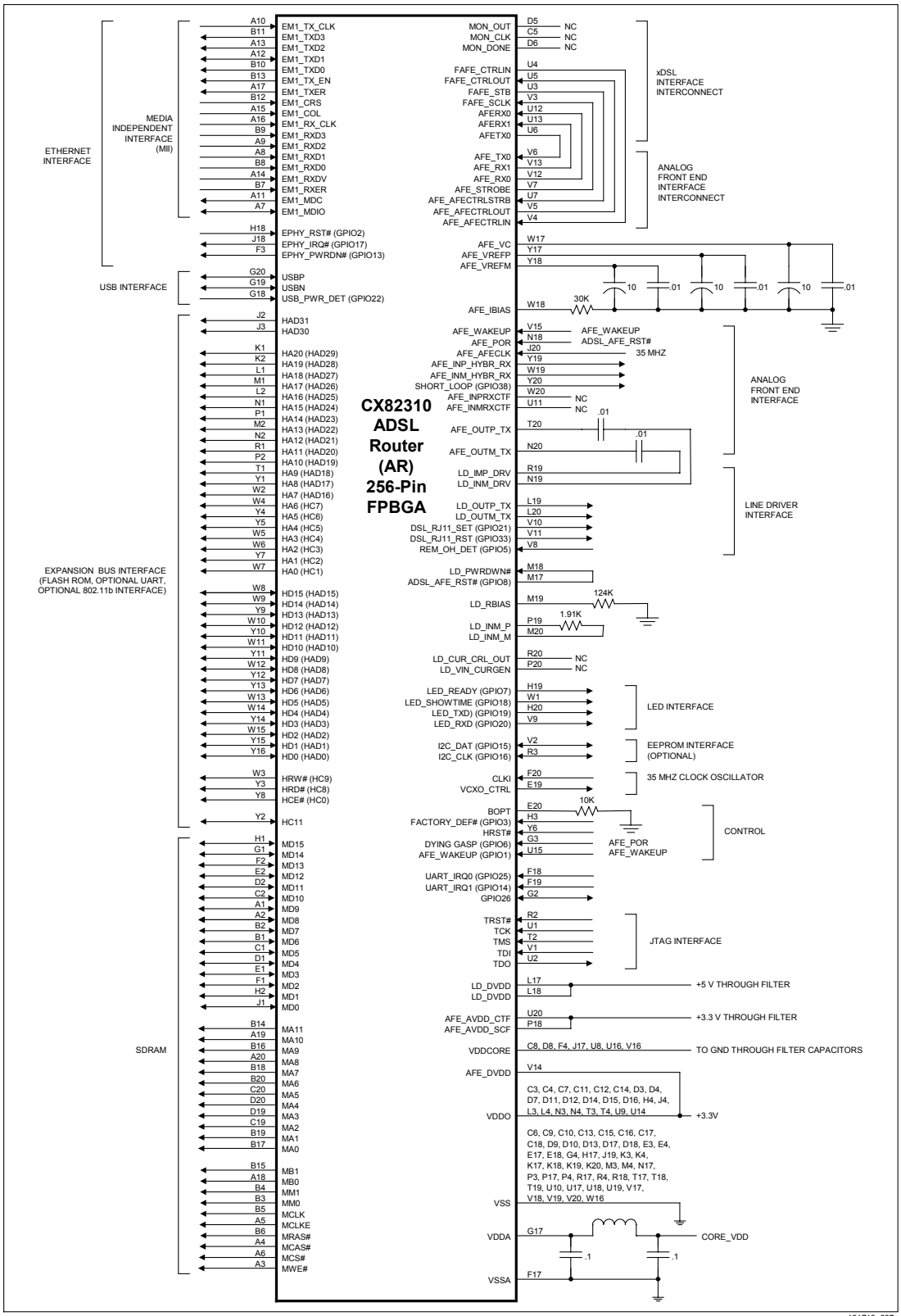
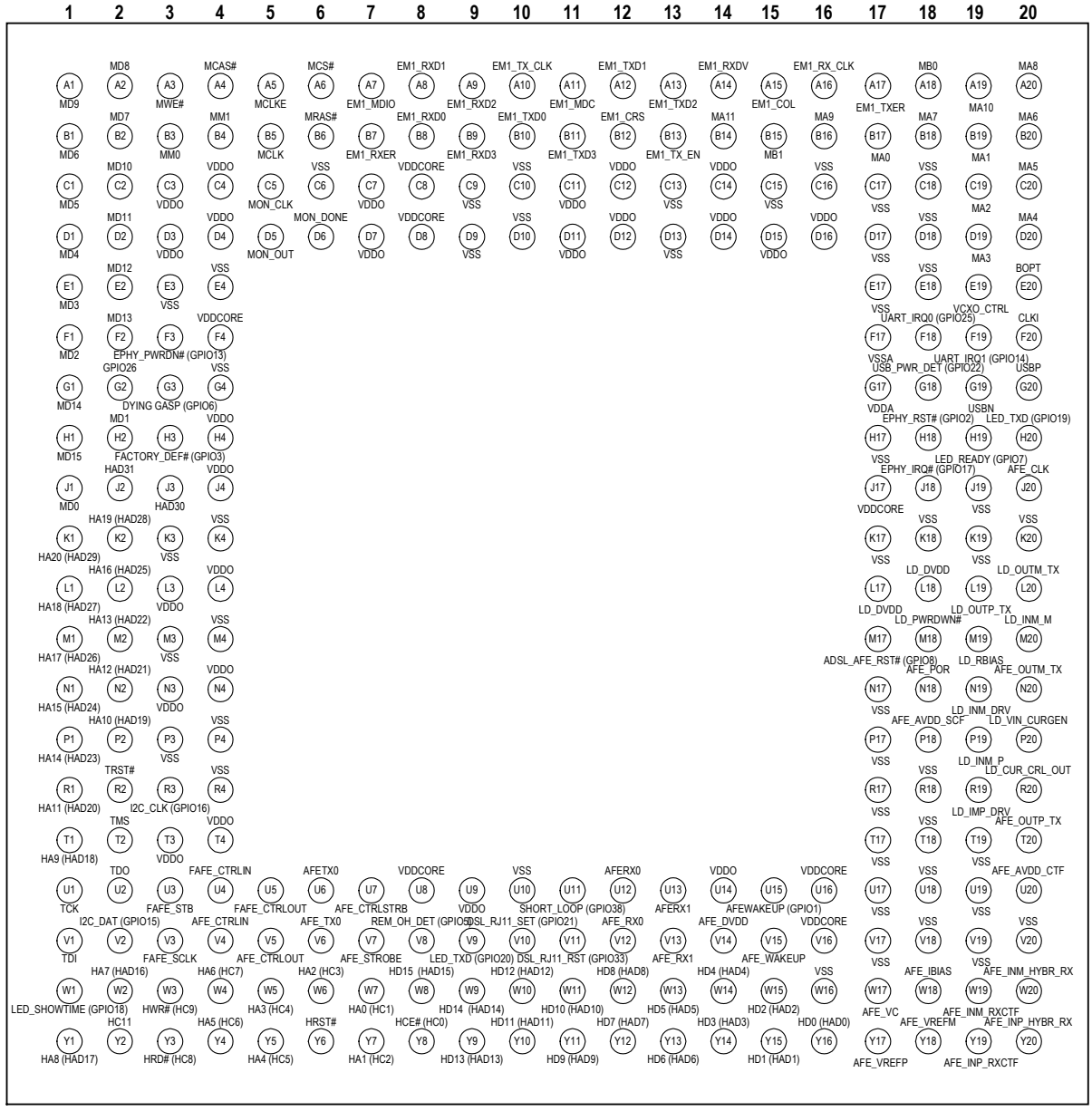


Figure 3-2. CX82310 ADSL Router Pin Signals-256-Pin FPBGA



TOP VIEW

101719_008

Table 3-1. CX82310 ADSL Router Hardware Signals

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	MD9	B13	EM1_TX_EN	D5	MON_OUT	G1	MD14
A2	MD8	B14	MA11	D6	MON_DONE	G2	GPIO26
A3	MWE#	B15	MB1	D7	VDDO	G3	DYING GASP (GPIO6)
A4	MCAS#	B16	MA9	D8	VDDCORE	G4	VSS
A5	MCLKE	B17	MA0	D9	VSS	G17	VDDA
A6	MCS#	B18	MA7	D10	VSS	G18	USB_PWR_DET (GPIO22)
A7	EM1_MDIO	B19	MA1	D11	VDDO	G19	USBN
A8	EM1_RXD1	B20	MA6	D12	VDDO	G20	USBP
A9	EM1_RXD2	C1	MD5	D13	VSS	H1	MD15
A10	EM1_TX_CLK	C2	MD10	D14	VDDO	H2	MD1
A11	EM1_MDC	C3	VDDO	D15	VDDO	H3	FACTORY_DEF# (GPIO3)
A12	EM1_TXD1	C4	VDDO	D16	VDDO	H4	VDDO
A13	EM1_TXD2	C5	MON_CLK	D17	VSS	H17	VSS
A14	EM1_RXDV	C6	VSS	D18	VSS	H18	EPHY_RST# (GPIO2)
A15	EM1_COL	C7	VDDO	D19	MA3	H19	LED_READY (GPIO7)
A16	EM1_RX_CLK	C8	VDDCORE	D20	MA4	H20	LED_TXD (GPIO19)
A17	EM1_TXER	C9	VSS	E1	MD3	J1	MD0
A18	MB0	C10	VSS	E2	MD12	J2	HAD31
A19	MA10	C11	VDDO	E3	VSS	J3	HAD30
A20	MA8	C12	VDDO	E4	VSS	J4	VDDO
B1	MD6	C13	VSS	E17	VSS	J17	VDDCORE
B2	MD7	C14	VDDO	E18	VSS	J18	EPHY_IRQ# (GPIO17)
B3	MM0	C15	VSS	E19	VCXO_CTRL	J19	VSS
B4	MM1	C16	VSS	E20	BOPT	J20	AFE_CLK
B5	MCLK	C17	VSS	F1	MD2	K1	HA20 (HAD29)
B6	MRAS#	C18	VSS	F2	MD13	K2	HA19 (HAD28)
B7	EM1_RXER	C19	MA2	F3	EPHY_PWRDN# (GPIO13)	K3	VSS
B8	EM1_RXD0	C20	MA5	F4	VDDCORE	K4	VSS
B9	EM1_RXD3	D1	MD4	F17	VSSA	K17	VSS
B10	EM1_TXD0	D2	MD11	F18	UART_IRQ0 (GPIO25)	K18	VSS
B11	EM1_TXD3	D3	VDDO	F19	UART_IRQ1 (GPIO14)	K19	VSS
B12	EM1_CRS	D4	VDDO	F20	CLKI	K20	VSS

Table 3-1. CX82310 ADSL Router Hardware Signals (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
L1	HA18 (HAD27)	R1	HA11 (HAD20)	U17	VSS	W9	HD14 (HAD14)
L2	HA16 (HAD25)	R2	TRST#	U18	VSS	W10	HD12 (HAD12)
L3	VDDO	R3	I2C_CLK (GPIO16)	U19	VSS	W11	HD10 (HAD10)
L4	VDDO	R4	VSS	U20	AFE_AVDD_CTF	W12	HD8 (HAD8)
L17	LD_DVDD	R17	VSS	V1	TDI	W13	HD5 (HAD5)
L18	LD_DVDD	R18	VSS	V2	I2C_DAT (GPIO15)	W14	HD4 (HAD4)
L19	LD_OUTP_TX	R19	LD_IMP_DRV	V3	FAFE_SCLK	W15	HD2 (HAD2)
L20	LD_OUTM_TX	R20	LD_CUR_CRL_OUT	V4	AFE_CTRLIN	W16	VSS
M1	HA17 (HAD26)	T1	HA9 (HAD18)	V5	AFE_CTRLOUT	W17	AFE_VC
M2	HA13 (HAD22)	T2	TMS	V6	AFE_TX0	W18	AFE_IBIAS
M3	VSS	T3	VDDO	V7	AFE_STROBE	W19	AFE_INM_RXCTF
M4	VSS	T4	VDDO	V8	REM_OH_DET (GPIO5)	W20	AFE_INM_HYBR_RX
M17	ADSL_AFE_RST# (GPIO8)	T17	VSS	V9	LED_RXD (GPIO20)	Y1	HA8 (HAD17)
M18	LD_PWRDWN#	T18	VSS	V10	DSL_RJ11_SET (GPIO21)	Y2	HC11
M19	LD_RBIAS	T19	VSS	V11	DSL_RJ11_RST (GPIO33)	Y3	HRD# (HC8)
M20	LD_INM_M	T20	AFE_OUTP_TX	V12	AFE_RX0	Y4	HA5 (HC6)
N1	HA15 (HAD24)	U1	TCK	V13	AFE_RX1	Y5	HA4 (HC5)
N2	HA12 (HAD21)	U2	TDO	V14	AFE_DVDD	Y6	HRST#
N3	VDDO	U3	FAFE_STB	V15	AFE_WAKEUP	Y7	HA1 (HC2)
N4	VDDO	U4	FAFE_CTRLIN	V16	VDDCORE	Y8	HCE# (HC0)
N17	VSS	U5	FAFE_CTRLOUT	V17	VSS	Y9	HD13 (HAD13)
N18	AFE_POR	U6	AFETX0	V18	VSS	Y10	HD11 (HAD11)
N19	LD_INM_DRV	U7	AFE_CTRLSTRB	V19	VSS	Y11	HD9 (HAD9)
N20	AFE_OUTM_TX	U8	VDDCORE	V20	VSS	Y12	HD7 (HAD7)
P1	HA14 (HAD23)	U9	VDDO	W1	LED_SHOWTIME (GPIO18)	Y13	HD6 (HAD6)
P2	HA10 (HAD19)	U10	VSS	W2	HA7 (HAD16)	Y14	HD3 (HAD3)
P3	VSS	U11	SHORT_LOOP (GPIO38)	W3	HWR# (HC9)	Y15	HD1 (HAD1)
P4	VSS	U12	AFERX0	W4	HA6 (HC7)	Y16	HD0 (HAD0)
P17	VSS	U13	AFERX1	W5	HA3 (HC4)	Y17	AFE_VREFP
P18	AFE_AVDD_SCF	U14	VDDO	W6	HA2 (HC3)	Y18	AFE_VREFM
P19	LD_INM_P	U15	AFE_WAKEUP (GPIO1)	W7	HA0 (HC1)	Y19	AFE_INP_RXCTF
P20	LD_VIN_CURGEN	U16	VDDCORE	W8	HD15 (HAD15)	Y20	AFE_INP_HYBR_RX

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
Ethernet PHY Media Independent Interface (MII)				
EM1_TX_CLK	A10	I	It	**Transmit Clock.** EM1_TX_CLK is sourced by the EPHY. It provides the timing reference for the transfer of EM1_TX_EN, EM1_TXD[3:0], and EM1_TXER signals to the EPHY. Connect to EPHY TXCLK pin.
EM1_TXD[3:0]	B11, A13, A12, B10	O	Otts4	**Transmit Data.** For MII interface, EM1_TXD[3:0] are the 4-bit parallel transmit data lines. EM1_TXD[3:0] is driven off the rising edge and sampled on the rising edge of EM1_TX_CLK. The entire transmitted frame data is presented by the EM1_TXD[3:0] signal lines, and commences on the first leading edge of EM1_TX_CLK subsequent to EM1_TX_EN assertion. For each EM1_TX_CLK period in which EM1_TX_EN is asserted, EM1_TXD[3:0] are accepted for transmission by the EPHY. All fields except for the FCS are transmitted with the least significant nibble first. The LSb of each nibble is placed on EM1_TXD0. Connect EM1_TXD[3:0] to EPHY TXD[3:0], respectively.
EM1_TX_EN	B13	O	Otts4	**Transmit Enable.** EM1_TX_EN is driven off the rising edge and sampled on the rising edge of EM1_TX_CLK. It indicates that the HNP is presenting nibbles on the MII for transmission. EM1_TX_EN is asserted when the HNP has data to transmit over the medium and remains asserted for the duration of the entire transmitted frame. The HNP de-asserts EM1_TX_EN prior to the rising edge of EM1_TX_CLK following the final nibble of a frame. Connect to EPHY TXEN pin.
EM1_TXER	A17	O	Otts4	**Transmit Error.** When EM1_TXER is asserted for one or more EM1_TX_CLK periods while EM1_TXEN is also asserted, the EPHY emits one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. Permissible encoding of EM1_TXER with EM1_TXEN and EM1_TXD[3:0] are: **EM1_TXEN / EM1_TXER / EM1_TXD[3:0] / Description** 0 / 0 / 0000–1111 / Normal Inter-Frame 0 / 1 / 0000–1111 / Reserved 1 / 0 / 0000–1111 / Normal Data Transmission 1 / 1 / 0000–1111 / Transmit Error Propagation Connect to EPHY TXER pin.
EM1_CRS	B12	I	It	**Carrier Sense.** In full-duplex mode, EM1_CRS is ignored. In half-duplex mode, EM1_CRS is asserted by the EPHY when either the transmit or receive medium is not idle. It is de-asserted by the EPHY when both the transmit and receive media are idle. The EPHY ensures that EM1_CRS remains asserted throughout the duration of a collision condition, i.e., when EM1_COL = 1. Connect to EPHY CRS pin.
EM1_COL	A15	I	It	**Collision Indication.** In full-duplex mode, EM1_COL is ignored. In half-duplex mode, EM1_COL is asserted by the EPHY upon detection of a collision on the medium, and remains asserted while the collision condition persists. Connect to EPHY COL pin.

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Ethernet PHY Media Independent Interface (MII) (Continued)				
EM1_RX_CLK	A16	I	It	**Receive Clock.** A 10 MHz square wave synchronized to the Receive Data and only active while receiving an input bit stream. EM1_RX_CLK is sourced by the EPHY. It provides the timing reference for the transfer of EM1_RXDV, EM1_RXD[3:0], and EM1_RXER signals from EPHY. The EPHY can either recover EM1_RX_CLK from the received data or it may derive EM1_RX_CLK from a nominal clock (e. g., the EM1_TX_CLK reference). If loss of received signal from the medium causes the EPHY to lose the recovered clock reference, the EPHY must source the clock from a nominal clock reference. Transitions from nominal clock to recovered clock or vice versa are made only when EM1_RXDV is de-asserted. During the interval between the assertion of EM1_CRS and the assertion of EM1_RXDV at the beginning of a frame, the EPHY may extend a cycle of EM1_RX_CLK by holding it either high or low until the EPHY has locked to the recovered clock. Following the de-assertion of EM1_RXDV at the end of a frame, the EPHY may extend a cycle of EM1_RX_CLK by holding it either high or low for an interval not to exceed twice the nominal clock period. Connect to EPHY RXCLK pin.
EM1_RXD[3:0]	B9, A9, A8, B8	I	Itpd	**Receive Data.** EM1_RXD[3:0] are the 4-bit parallel receive data lines. Connect EM1_RXD[3:0] to EPHY RXD[3:0], respectively.
EM1_RXDV	A14	I	Ipd	**Receive Data Valid.** EM1_RXDV is asserted by the EPHY to indicate that the nibble on EM1_RXD[3:0] is valid. It remains asserted for the received frame duration with the exception of the preamble. It may or may not be asserted during the preamble. EM1_RXDV is de-asserted prior to the first EM1_RX_CLK period that follows the final nibble of a received frame. When EM1_RXDV is de-asserted, the EMAC ignores EM1_RXD[3:0]. Connect to EPHY RXDV.
EM1_RXER	B7	I	Itpd	**Receive Error.** EM1_RXER is driven by the EPHY. It is asserted for one or more EM1_RX_CLK periods to indicate that an error was detected somewhere in the frame presently being transferred from the EPHY. The RMAC hardware will detect this condition and declare such a frame invalid. While EM1_RXDV is deasserted, EM1_RXER has no effect on the Reconciliation sublayer (which lies between the MII and the MAC), therefore, it has no effect on the MAC as well. Connect to EPHY RXER pin.
EM1_MDC	A11	I/O	Otts4	**Management Data Clock.** EM1_MDC is sourced by the Station Management entity (STA) of the EMAC as the timing reference for transfer of information on the EM1_MDIO signal. EM1_MDC is aperiodic and has no maximum high or low times. The minimum high and low time for EM1_MDC is 160 ns each. The minimum period for EM1_MDC is 400 ns.
EM1_MDIO	A7	I/O	Itpd/Ot4	**Serial Management Data Input/Output.** EM1_MDIO is a bidirectional signal used to transfer control and status information between the EPHY and the STA in the EMAC.
EPHY_RST# (GPIO2)	H18	O	Itpu/Ot4	**Ethernet Reset**. Active low output used to reset the EPHY. Optionally (usually through a 0 Ω resistor), connect to the EPHY nRST pin, to +3.3 V though 10 KΩ, and to GND though 1 KΩ and 4.7 μF in parallel.

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Ethernet PHY Media Independent Interface (MII) (Continued)				
EPHY_IRQ# (GPIO17)	J18	I	Itpu/Ot4	**Ethernet Interrupt Request**. Active low input used to request interrupt service for the EPHY. Optionally (usually through a 0 Ω resistor), connect to the EPHY nINTR pin.
EPHY_PWRDN# (GPIO13)	F3	O	Itpu/Ot4	**Ethernet Power Down**. Active low output used to power down the EPHY. Optionally (usually through a 0 Ω resistor), connect to the EPHY PWRDN pin.
DSL Interface –Test Monitor				
MON_OUT	D5	O	Ot4	**Monitor Output.** 1-bit serial D/A output used for constellation monitoring. Used for test only. Leave open during normal operation.
MON_CLK	C5	O	Ot4	**Monitor Clock.** Serial monitor 138 kHz clock output. Used for test only. Leave open during normal operation.
MON_DONE	D6	O	Ot4	**Monitor Done.** New symbol constellation qualifier. Used for test only. Leave open during normal operation.
DSL Interface – CX82310 DSL/AFE Interface Interconnect				
FAFE_CTRLIN	U4	O	Ot4	**AFE Control In.** Serial control data output to the CX82310 AFE Interface. Connect to CX82310 AFE_CTRLIN.
FAFE_CTRLOUT	U5	I	It	**AFE Control Out.** Serial control data input from the CX82310 AFE Interface. Connect to CX82310 AFE_CTRLOUT.
FAFE_STB	U3	O	Ot4	**AFE Control Strobe.** Control data strobe output to the CX82310 AFE Interface. Connect to CX82310 AFE_CTRLSTRB.
FAFE_SCLK	V3	I	It	**AFE Data Strobe.** Data strobe input from the CX82310 AFE Interface. The negative edge triggers the transfer of serial transmit data on TX0 to the CX82310 AFE Interface and triggers the transfer of serial receive data on RX0 and RX1 from the CX82310 AFE Interface. Connect to CX82310 AFE_STROBE.
AFETX0	U6	O	Ot4	**AFE Transmit Data.** Serial transmit data output to the CX82310 AFE Interface. The negative edge of the AFE_STROBE signal from the CX82310 AFE Interface clocks the data out of the CX82310 DSL Interface. Connect to CX82310 AFE_TX0.
AFERX0	U12	I	It	**AFE Receive Data.** Serial receive data input from the CX82310 AFE Interface. The negative edge of the AFE_STROBE signal from the CX82310 AFE Interface clocks the data into the CX82310 DSL Interface. Connect to CX82310 AFE_RX0.
AFERX1	U13	I	It	**AFE Receive Data.** Serial receive data input from the CX82310 AFE Interface. The negative edge of the AFE_STROBE signal from the CX82310 AFE Interface clocks the data into the CX82310 DSL Interface. Connect to CX82310 AFE_RX1.

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
AFE Interface – CX82310 DSL/AFE Interface Interconnect				
AFE_CTRLIN	V4	I	It	**AFE Control In.** Serial control data input from the CX82310 DSL Interface. Connect to CX82310 FAFE_CTRLIN.
AFE_CTRLOUT	V5	O	Ot4	**AFE Control Out.** Serial control data output to the CX82310 DSL Interface. Connect to CX82310 FAFE_CTRLOUT.
AFE_CTRLSTRB	U7	I	It	**AFE Control Strobe.** Control data strobe input from the CX82310 DSL Interface. Connect to CX82310 FAFE_STB.
AFE_STROBE	V7	O	Ot4	**AFE Data Strobe.** Data strobe output to the CX82310 DSL Interface. The negative edge triggers the transfer of serial transmit data on TX0 from the CX82310 DSL Interface and triggers the transfer of serial receive data on RX0 and RX1 to the CX82310 DSL Interface. Connect to CX82310 FAFE_SCLK.
AFE_TX0	V6	I	It	**AFE Transmit Data**. Serial transmit data input from the CX82310 DSL Interface. The negative edge of the AFE_STROBE signal clocks the data out of the CX82310 DSL Interface. Connect to CX82310 AFETX0.
AFE_RX0	V12	O	Ot4	**AFE Receive Data.** Serial receive data output to the CX82310 DSL Interface. The negative edge of the AFE_STROBE signal clocks the data into the CX82310 DSL Interface. Connect to CX82310 AFERX0.
AFE_RX1	V13	O	Ot4	**AFE Receive Data.** Serial receive data output to the CX82310 DSL Interface. The negative edge of the AFE_STROBE signal clocks the data into the CX82310 DSL Interface. Connect to CX82310 AFERX1.
AFE Interface – Reference Voltages				
AFE_VC	W17	R	REF	**Analog Reference Voltage (+1.5V)**. Connect to GND through 10 μF and 0.1 μF in parallel.
AFE_VREFP	Y17	R	REF	**Analog Reference Voltage (+2.5V)**. Connect to GND through 10 μF and 0.1 μF in parallel.
AFE_VREFM	Y18	R	REF	**Analog Reference Voltage (+0.5V)**. Connect to GND through 10 μF and 0.1 μF in parallel.
AFE_IBIAS	W18	R	REF	**Analog Current Reference.** Current setting external resistor. Connect to GND through 30 KΩ (±1%).
AFE Interface – Control and Test				
AFE_WAKEUP	V15	O	Ot	**Wakeup.** Digital output for tone detection mode. Connect to CX82310 AFEWAKEUP (GPIO1) through a 0 Ω resistor.
AFE_POR	N18	I	It	**Reset.** Active low power-on reset. Connect to CX82310 ADSL_AFE_RST#.
AFE_CLK	J20	I	Ith	**AFE Clock In.** Connect to 35.328 MHz voltage controlled crystal oscillator (VCXO) output through 51 Ω.
AFE_INMRXCTF	W19			Typically, connect to test point (e.g., TV1).
AFE_INPRXCTF	Y19			Typically, connect to test point (e.g., TV2).

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
AFE Interface – Hybrid Interface				
AFE_INM_HYBR_RX	W20	I	Iafe	**Receive Input Negative from Hybrid.** Receive input negative AC coupled from the hybrid circuit.
AFE_INP_HYBR_RX	Y20	I	Iafe	**Receive Input Positive from Hybrid.** Receive input positive AC coupled from the hybrid circuit.
SHORT_LOOP (GPIO38)	U11	O	It/Ot4	**Short Loop Relay Control.** Active low output used to control short loop relay circuit. Optionally, connect to short loop relay circuit.
AFE Interface – CX82310 Line Driver Interface Interconnect				
AFE_OUTP_TX	T20	O	Oa	**Transmit Output Positive.** Transmit output positive to the LD. Connect to CX82310 LD_INP_DRV through 1 µF.
AFE_OUTM_TX	N20	O	Oa	**Transmit Output Negative.** Transmit output negative to the LD. Connect to CX82310 LD_INM_DRV through 1 µF.
Line Driver Interface – CX82310 AFE Interface Interconnect				
LD_INP_DRV	R19	I	Iald	**Input Driver Positive.** Transmit driver input positive from the AFE. Connect to CX82310 AFE_OUTP_TX through 1 µF.
LD_INM_DRV	N19	I	Iald	**Input Driver Negative.** Transmit driver input negative input from the AFE. Connect to CX82310 AFE_OUTM_TX through 1 µF.
Line Driver Interface – External Line Driver Interface				
LD_OUTP_TX	L19	O	Oa	**Output Driver Positive.** Transmit driver output positive to the hybrid circuit. I_{max} = 280 mA. Connect to external Line Driver LD_OUTM_TX.
LD_OUTM_TX	L20	O	Oa	**Output Driver Negative.** Transmit driver output negative to the hybrid circuit. I_{max} = 280 mA. Connect to external Line Driver LD_OUTP_TX.
DSL_RJ11_SEL (GPIO21)	V10	O	Itpu/Ot4	**Inner/Outer Pair Select Set.** Optionally, connect to line select option, auto sense relay circuit.
DSL_RJ11_RST (GPIO31)	V11	O	Itpu/Ot4	**Inner/Outer Pair Select Reset.** Optionally, connect to line select option, auto sense relay circuit.
REM_OH_DET (GPIO5)	V8	I	It/Ot4	**Remote Off-Hook Detect.** Active low input used to indicate POTS off-hook event. Used for G.lite Mode only. Optionally, connect to off-hook detector circuit.
Line Driver Interface – Control and Test				
LD_PWRDWN#	M18	I	It	**Power Down.** Active low power down control input. Connect to CX82310 ADSL_AFE_RST#.
LD_RBIAS	M19	R	REF	**Bias.** Current setting external resistor. Connect to GND through 124 KΩ (±1%).
LD_INM_P	P19			Connect to CX82310 LD_INM_M through an **unpopulated** 1.91 KΩ resistor.
LD_INM_M	M20			Connect to CX82310 LD_INM_P through an **unpopulated** 1.91 KΩ resistor.
LD_CUR_CRL_OUT	R20			**Not Used.** Typically, connect to test point (e.g., TV5).
LD_VIN_CURGEN	P20			**Not Used.** Typically, connect to test point (e.g., TV6).

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Expansion Bus Interface (Described for Flash ROM Connection)				
HA[20:7] (HAD[29:16])	K1, K2, L1, M1, L2, N1, P1, M2, N2, R1, P2, T1, Y1, W2	O	Ot4	**Address Lines 20-7.** Connect HA[20:7] (HAD[29:16]) to Flash ROM A[20:7], respectively.
HA[6:0] (HC[07:01])	W4, Y4, Y5, W5, W6, Y7, W7	O	Ot4	**Address Lines 6-0.** Connect HA[6:0] (HC[07:01]) to Flash A[6:0], respectively.
HD[15:0] (HAD[15:0])	W8, W9, Y9, W10, Y10, W11, Y11, W12, Y12, Y13, W13, W14, Y14, W15, Y15, Y16	I/O	It/Ot4	**Data Lines 15-00.** Connect HD[15:0] (HAD[15:0]) to Flash D[15:0], respectively.
HWR# (HC09)	W3	O	Ot4	**Write Enable.** Active low write enable. When asserted, data is transferred from the data bus into the selected Flash ROM. Connect to Flash ROM WE#.
HRD# (HC08)	Y3	O	Ot4	**Read Enable.** Active low read enable. When asserted, data is transferred from the selected Flash ROM onto the data bus. Connect to Flash ROM OE#.
HCE# (HC00)	Y8	O	Ot4	**Flash ROM Chip Enable.** Active low output enables Flash ROM when asserted. Connect to Flash ROM CE#.
HAD[31:30]	J2, J3	I/O	It/Ot4	**Not Used.** Typically, connect to a test point (e.g., TV8 and TV7, respectively) or leave open.
HC11	Y2	I/O	Itpd/Ot4	**Not Used.** Typically, connect to test point (e.g., TV9).

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
SDRAM Interface				
MD[15:00]	H1, G1, F2, E2, D2, C2, A1, A2, B2, B1, C1, D1, E1, F1, H2, J1	I/O	It/Ot4	**Data Lines.** Connect MD[15:00] to SDRAM DQ[15:0], respectively, each line through 51 Ω.
MA[11:00]	B14, A19, B16, A20, B18, B20, C20, D20, D19, C19, B19, B17	O	Ot4	**Multiplexed Row and Column Address Lines.** For 2MB SDRAM, Connect MA[10:00] to SDRAM A[10:0], respectively, each line through 51 Ω. For 8MB SDRAM, Connect MA[11:00] to SDRAM A[11:0], respectively, each line through 51 Ω.
MM1	B4	O	Ot4	**Input/Output Mask 1.** Connect to SDRAM I/O Mask High input (DQMH).
MM0	B3	O	Ot4	**Input/Output Mask 0.** Connect to SDRAM I/O Mask Low input (DQML).
MB1	B15	O	Ot4	**Bank Address Select 1.** Connect to SDRAM Bank Address Select 1 input (BA1).
MB0	A18	O	Ot4	**Bank Address Select 0.** For 2 MB SDRAM, leave open. For 8 MB SDRAM; connect to SDRAM/SRAM Bank Address Select 0 input (BA0).
MCLK	B5	O	Ot4	**SDRAM Clock.** Connect to SDRAM Clock input (CLK) through 51 Ω.
MCLKE	A5	O	Ot4	**SDRAM Clock Enable.** Active high; enables SDRAM clock. Connect to SDRAM Clock Enable input (CLKE).
MRAS#	B6	O	Ot4	**SDRAM Row Address Strobe.** Active low; starts SDRAM access with strobe of row address. Connect to SDRAM RAS input (RAS#) through 51 Ω.
MCAS#	A4	O	Ot4	**SDRAM Column Address Strobe.** Active low; strobes column address and data bytes. Connect to SDRAM CAS input (CAS#) through 51 Ω.
MWE#	A3	O	Ot4	**SDRAM Memory Write Enable.** Active low; indicates write access to SDRAM. Connect to SDRAM Write Enable input (WE#) through 51 Ω.
MCS#	A6	O	Ot4	**SDRAM Memory Chip Select.** Active low; enables SDRAM command decoder. Connect to SDRAM chip select input (CS#) through 51 Ω.
USB Interface				
USBP USBN	G20 G19	I/O	Iu/Ou	**USB Port**. USBP and USBN are the differential data positive and negative signals of the USB port. Connect USBP and USBN to USB +Data and -Data, respectively, each line through 24 Ω.
USB5V_DET (GPIO22)	G18	I	It	**USB 5 V Detect.** Active high input used to detect presence of +5 V at the USB connector.

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
LED Interface				
LED_READY (GPIO7)	H19	O	Ot4	**Ready LED.** Active high output used to illuminate an LED when the device is successfully enumerated on the USB. Optionally, connect to an LED circuit.
LED_SHOWTIME (GPIO18)	W1	O	Ot4	**Showtime LED.** Active high output used to illuminate an LED when the ADSL transceiver is in Showtime Mode. Optionally, connect to an LED circuit.
LED_TXD (GPIO19)	H20	O	Ot4	**ADSL Transmit Data LED.** Active high output used to illuminate an LED when data is transmitted to the ADSL line. Optionally, connect to an LED circuit.
LED_RXD (GPIO20)	V9	O	Ot4	**ADSL Receive Data LED.** Active high output used to illuminate an LED when data is received from the ADSL line. Optionally, connect to an LED circuit.
Serial EEPROM Interface (Optional)				
I2C_DAT (GPIO15)	V2	I/O	Itpu/Ot4	**Serial EEPROM Data.** I2C_DAT is a bidirectional data line used to transfer data into and out of the EEPROM. Connect to the EEPROM SDA pin and to +3.3V through 4.7K Ω.
I2C_CLK (GPIO16)	R3	O	Itpu/Ot4	**Serial EEPROM Shift Clock**. The I2C_CLK output is used to clock all data into and out of the EEPROM. Connect to the EEPROM SCL pin and to +3.3V through 4.7K Ω.
JTAG Interface				
TRST#	R2	I	Itpu	**JTAG Reset.** A high-to-low transition on this signal forces the TAP controller into a logic reset state. This pin has an internal pullup, and it conforms to IEEE 1149.1 JTAG specification.
TCK	U1	I	It	**JTAG Test Clock.** This is the boundary scan clock input signal. This pin has an internal pullup, and it conforms to IEEE 1149.1 JTAG specification.
TMS	T2	I	Itpu	**JTAG Test Mode Select.** This signal controls the operation of the TAP controller. This pin has an internal pull-up, and it conforms to IEEE 1149.1 JTAG specification.
TDI	V1	I	Itpu	**JTAG Test Input.** This signal contains serial data that is shifted in on the rising edge of TCK. The pin has an internal pullup, and it conforms to IEEE 1149.1 JTAG specification.
TDO	U2	O	Otts4	**JTAG Test Output Data.** This is the three-stateable boundary scan data output signal from the MCU, and it is shifted out on the falling edge of TCK. It conforms to IEEE 1149.1 JTAG specification.

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Clock Interface				
CLKI	F20	I	Ith	**Clock In.** Connect to 35.328 MHz voltage controlled crystal oscillator (VCXO) output.
VCXO_CTRL	F19	O	Ot4	**VCXO Control Out.** Oversampled VCXO analog control voltage output. Connect to VCXO control circuit.
CX82310 Control and Monitor Interconnect				
BOPT	E20	I	It	**Boot Option.** To boot from internal ROM, leave open. To boot from external Flash ROM (normal operation), connect to GND through 10 KΩ. For in-circuit programming of the Flash ROM, BOPT must be connected to +3.3 V during power-up.
HRST#	Y6	I	Ith	**Reset.** Active low input signal to reset the CX82310. Typically, connect to an RC reset circuit, which can optionally be part of a dying gasp circuit.
FACTORY_DEF# (GPIO3)	H3	I	It/Ot4	**Factory Default.** Active low input used to initialize the CX82310 to factory default values. Typically, connect to the switch to GND.
DYING GASP (GPIO6)	G3	I	It/Ot4	**Dying Gasp.** Active high input used to inform the CX82310 of loss of power. Upon assertion in a typical dying gasp circuit, software must be initialized and completed with 75 ms. If not used, connect to GND.
ADSL_AFE_RST# (GPIO8)	M17	O	It/Ot4	**AFE and LD Reset.** Active low output used to reset the CX82310 the AFE circuit and to power down the CX82310 LD circuit. Connect to CX82310 AFE_POR and to CX82310 LD_PWRDN.
AFE_WAKEUP (GPIO1)	U15	I	Ith/Ot4	**AFE Wakeup.** Active low input used for DSL power management. Connect to CX82310 AFE_WAKEUP through a 0 Ω resistor.
UART_IRQ0 (GPIO25)	F18	I	Ith/Ot4	**UART Interrupt Request 0.** Active low input used to request interrupt service for the UART port. Used for factory test only. Connect to GND through 4.7 KΩ for normal operation.
UART_IRQ1 (GPIO14)	F19	I	Ith/Ot4	**UART Interrupt Request 1.** Active low input used to request interrupt service for the UART port. Used for factory test only. Connect to GND through 4.7 KΩ for normal operation.
GPIO26	G2	I/O	It/Ot4	**General Purpose Input/Output 26.** Not used. Leave open.

Table 3-2. CX82310 ADSL Router Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Power and Ground				
AFE_AVDD_CTF AFE_AVDD_STF	U20 P18	P	PWR	**+3.3 V AFE Analog Circuits Supply Voltage.** Connect to +3.3 V through LC filter.
AFE_DVDD_CTF	V14	P	PWR	**+3.3 V AFE Digital Circuits Supply Voltage.** Connect to +3.3 V.
LD_DVDD	L17, L18	P	PWR	**+5 V Line Driver Supply Voltage.** Connect to +5 V through LC filter.
VDDCORE	C8, D8, F4, J17, U8, U16, V16	P	PWR	**Core Voltage Filter Capacitors Connection**. Connect to digital ground through filter capacitors.
VDDO	C3, C4, C7, C11, C12, C14, D3, D4, D7, D11, D12, D14, D15, D16, H4, J4, L3, L4, N3, N4, T3, T4, U9, U14	P	PWR	**I/O Supply Voltage.** Connect to +3.3V.
VSS	C6, C9, C10, C13, C15, C16, C17, C18, D9, D10, D13, D17, D18, E3, E4, E17, E18, G4, H17, J19, K3, K4, K17, K18, K19, K20, M3, M4, N17, P17, P4, R17, R4, R18, T17, T18, T19, U10, U17, U18, U19, V17, V18, V19, V20, W16	G	GND	**Ground.** Connect to digital ground.
VDDA	G17	P	PWR	**+1.8 V Analog Supply Voltage.** Connect to CX82310 VDDCORE pins through LC filter.
VSSA	F17	G	GND	**+1.8 V Analog Supply Ground.** Connect to digital ground.
NOTES: I/O Types: See Table 3-5.				

3.2 Hardware Signal Definitions for Optional 802.11b Interface

The host bus can be connected to an 802.11b interface for Wireless ADSL router applications. The interface connections are illustrated in Figure 3-3. Interface logic operation is listed in Table 3-3. This logic can be implemented in a single inverter and a quad OR gate.

The interface signals are defined in Table 3-4. GPIO signals that are used for the 802.11b interface are identified with 802.11b interface signal labels.

Figure 3-3. Hardware Interface Signals for 802.11b Interface

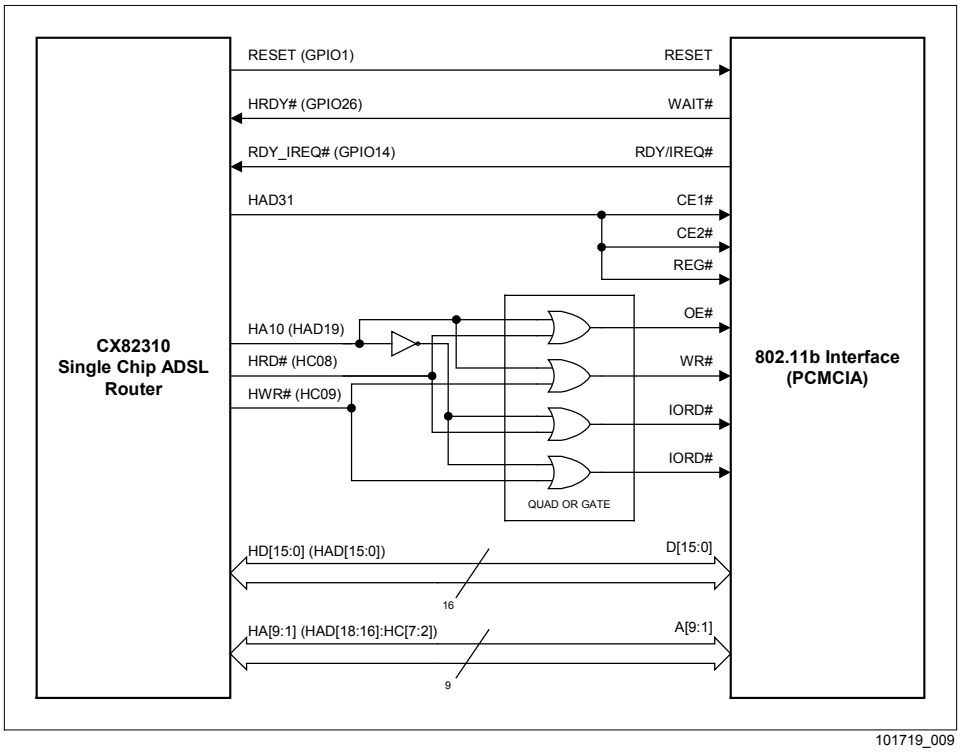


Table 3-3. Hardware Signal Interface Logic for 802.11b Interface

CX832100 Pin Signals		802.11b Interface Signals through Logic	
HA10 (HAD19)	**HRD# (HC8)**	**OE#**	**IORD#**
H	H	H	H
H	L	H	L
L	H	H	H
L	L	L	H
HA10 (HAD19)	**HWR# (HC9)**	**WR#**	**IOWR#**
H	H	H	H
H	H	H	L
L	H	H	H
L	L	L	H

Table 3-4. CX82310 ADSL Router Hardware Signal Definitions for 802.11b Interface

Label	Pin	I/O	I/O Type	Signal Name/Description
802.11b Interface (Optional)				
RESET (GPIO1)	U15	O	Ith/Ot4	**Reset.** Active high output asserted to reset the 802.11b interface. Connect to RESET on the 802.11b interface device.
HRDY# (GPIO26)	G2	I	It/Ot4	**Wait.** Active low input asserted to indicate that the 802.11b interface is ready. Connect to WAIT# on the 802.11b interface.
RDY_IREQ# (GPIO14)	F19	I	Ith/Ot4	**Ready or Interrupt Request.** Active low input asserted to indicate that the 802.11b interface device is ready or is requesting interrupt service. Connect to RDY_IREQ# on the 802.11b interface device.
HAD31	J2	O	It/Ot4	**Chip Enable and Register Select & I/O Enable.** Active low output asserted to enable the 802.11b interface. Connect to CE1#, CE2# and REG# on the 802.11b interface.
HA10 (HAD19)	P2	O	Ot4	**Output Enable.** Active low output asserted to enable data to be read from the 802.11b interface. Connect to OE#, WR#, IORD#, and IOWR# on the 802.11b interface through logic.
HRD# (HC08)	Y3	O	Ot4	**Read Enable.** Active low output asserted to read data from the 802.11b interface. Connect to IORD# on the 802.11b interface through logic.
HWR# (HC09)	W3	O	Ot4	**Write Enable.** Active low output asserted to write data to the 802.11b interface. Connect to IOWR# on the 802.11b interface though logic.
HA[9:1] (HAD[18:16], HC[07:02])	T1, Y1, W2, W4, Y4, Y5, W5, W6, Y7,	O	Ot4	**Address Lines 9-1.** Connect HA[9:1] (HAD[18:16], HC[07:02]) to A[9:1], respectively, on the 801.11b interface.
HD[15:0] (HAD[15:0])	W8, W9, Y9, W10, Y10, W11, Y11, W12, Y12, Y13, W13, W14, Y14, W15, Y15, Y16	I/O	It/Ot4	**Data Lines 15-0.** Connect HD[15:0] (HAD[15:0]) to D[15:0], respectively, on the 801.11b interface.

3.3 CX82310 ADSL Router Electrical and Environmental Specifications

CX82310 ADSL Router input/output type descriptions are listed Table 3-5.

CX82310 ADSL Router DC electrical characteristics are listed Table 3-6.

CX82310 ADSL Router operating conditions are specified in Table 3-7.

CX82310 ADSL Router absolute maximum ratings are stated in Table 3-8.

CX82310 ADSL Router power consumption is listed in Table 3-9.

Table 3-5. CX82310 ADSL Router Input/Output Type Descriptions

I/O Type	Description
Iafe	Analog input (see analog electrical characteristics in Table 3-10)
Iald	Analog input (see analog electrical characteristics in Table 3-11)
It	Digital input, +3.3V tolerant, C_{IN} = 8 pF
It/Ot4	Digital input, +3.3V tolerant, C_{IN} = 8 pF/Digital output, 4 mA, Z_{INT} = 80 Ω
Ith	Digital input, +3.3V tolerant, with hysteresis, C_{IN} = 8 pF
Itpd	Digital input, +3.3V tolerant, 75k Ω pull-down, C_{IN} = 8 pF
Itpu	Digital input, +3.3V tolerant, 75k Ω pull-up, C_{IN} = 8 pF
Itpu/Ot4	Digital input, +3.3V tolerant, 75k Ω pull-up, C_{IN} = 8 pF/Digital output, 4 mA, Z_{INT} = 80 Ω
Oafe	Analog output (see analog electrical characteristics in Table 3-10)
Oald	Analog output (see analog electrical characteristics in Table 3-11)
Otts4	Digital output, 3-State, 4 mA, Z_{INT} =80 Ω
Iu/Ou	Input, USB receiver/Output, USB driver

NOTES:

1. See DC characteristics in Table 3-6.
2. I/O Type corresponds to the device Pad Type. The I/O column in tables refers to signal I/O direction used in the application.

Table 3-6. CX82310 ADSL Router DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input high voltage	VIH	2.0		VGG + 0.5	VDC	
Input low voltage	VIL	-0.5		0.8	VDC	
Input leakage current	IIL/IIH	-10		10	µA	VIN = 0 for Min. VIN = VIN (MAX) for Max.
Input leakage current (with internal pull-downs)[2]	IIL/IIH	-10		100	µA	VIN = 0 for Min. VIN = VIN (MAX) for Max.
Input leakage current (with internal pull-ups)[2]	IIL/IIH	-100		10	µA	VIN = 0 for Min. VIN = VIN (MAX) for Max.
Internal pullup/pulldown resistance	Rpu/Rpd	50		200	kΩ	
Output high voltage	VOH	2.4		VDDO	VDC	IOH = 4 mA
Output low voltage	VOL			0.4	VDC	IOL = 4 mA
Input/output capacitance	CINOUT		3		pF	

NOTES:

1. Test Conditions (unless otherwise stated):
   VDDcore = +1.8 ± 0.15 VDC
   VDDO = +3.3 ± 0.3 VDC;
   $V_{IN\ (MAX)}$ = +3.6V for VGG connected to +3.3V;
   $V_{IN\ (MAX)}$ = +5.25V for VGG connected to +5V.
2. Current flow out of the device is shown as minus.
3. Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table 3-7. CX82310 ADSL Router Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage	VDDO	3.0	3.3	3.6	VDC
Operating ambient temperature	TA	0		70	°C

Table 3-8. CX82310 ADSL Router Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage	VDDO	-0.35	3.7	VDC
Input voltage	VIN	-0.35	LD_DVDD + 0.35*	VDC
Voltage applied to outputs in high impedance (Off) state	VHZ	-0.35	LD_DVDD + 0.35*	VDC
Storage temperature	TS	-55	125	°C
* LD_DVDD = +5 V ± 0.5 VDC.				

Caution: Handling CMOS Devices

These devices contain circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage.

An unterminated input can acquire unpredictable voltages through coupling with stray capacitance and internal cross talk. Both power dissipation and device noise immunity degrades. Therefore, all inputs should be connected to an appropriate supply voltage.

Input signals should never exceed the voltage range from 0.5V or more negative than GND to 0.5V or more positive than VDD. This prevents forward biasing the input protection diodes and possibly entering a latch up mode due to high current transients.

Table 3-9. CX82310 ADSL Router Power Requirements

Mode	Typical Current (mA)	Typical Power (mW)	Maximum Power (mW)
VDDO	250 mA	825 mW	900 mW
LD_VDD	45 mA	225 mW	248 mW

NOTES:

1. Operating voltage: VDDO = +3.3 VDC ± 0.3 VDC.
   LD_VDD = +5 VDC ± 0.5 VDC.

2. Test conditions: VDDO = +3.3 VDC for typical values;
   VDDO = +3.6 VDC for maximum values.

   LD_VDD = +5 VDC for typical values;
   LD_VDD = +5.5 VDC for maximum values.

Table 3-10. CX82310 AFE Analog Electrical Characteristics

Parameter	Min.	Typ.	Max.	Units
Receive Path				
Differential input amplitude of in-band signal			2	Vp
Differential input amplitude of echo			2.1	Vp
Input-referred noise density in 170 kHz – 1104 kHz, gain = 27 dB		15	20	nV/sqrt (Hz)
Input-referred noise density in 170 kHz – 1104 kHz, gain = 0 dB		150		nV/sqrt (Hz)
Intermodulation product falling in the downstream band, from an echo tone with an in band signal, gain = 27 dB		-80		dBFS
Intermodulation product falling in the downstream band, from 2 in band tones, gain = 0 dB		-80		dBFS
In-band ripple		1.5		dB
Input resistance (single-ended)	85			kΩ
Input capacitance (single-ended)			90	pF
Transmit Path				
Differential output amplitude		2		Vp
Output-referred noise density in 25 kHz – 132 kHz		250	300	nV/sqrt (Hz)
Output-referred noise density in 170 kHz – 1104 kHz		20		nV/sqrt (Hz)
Intermodulation product from 2 in band tones		-80		dBV
In-band ripple		1.25		dB
Output resistive load (single-ended)	5	20		kΩ
Output capacitive load (single-ended)			20	pF

Table 3-11. CX82310 LD Analog Electrical Characteristics

Parameter	Min	Typ	Max	Units
Differential output amplitude			4.485	Vp
Differential input amplitude			2.0	Vp
Input signal bandwidth		25..132		kHz
Input referred noise density in 170 kHz – 1104 kHz		5	10	nV/sqrt (Hz)
Input referred noise density beyond 1104 kHz			270	nV/sqrt (Hz)
Intermodulation product falling in the downstream band from two in-band tones (100 kHz and 120 kHz)		-75		dBV
Differential gain		7.014		dB
In-band ripple			0.05	dB
Input capacitance (single-ended)			15	pF
Input resistance (single-ended)	20			kΩ
Output capacitance (single-ended)			10	pF
Output resistive load (single-ended)		18.36		Ω

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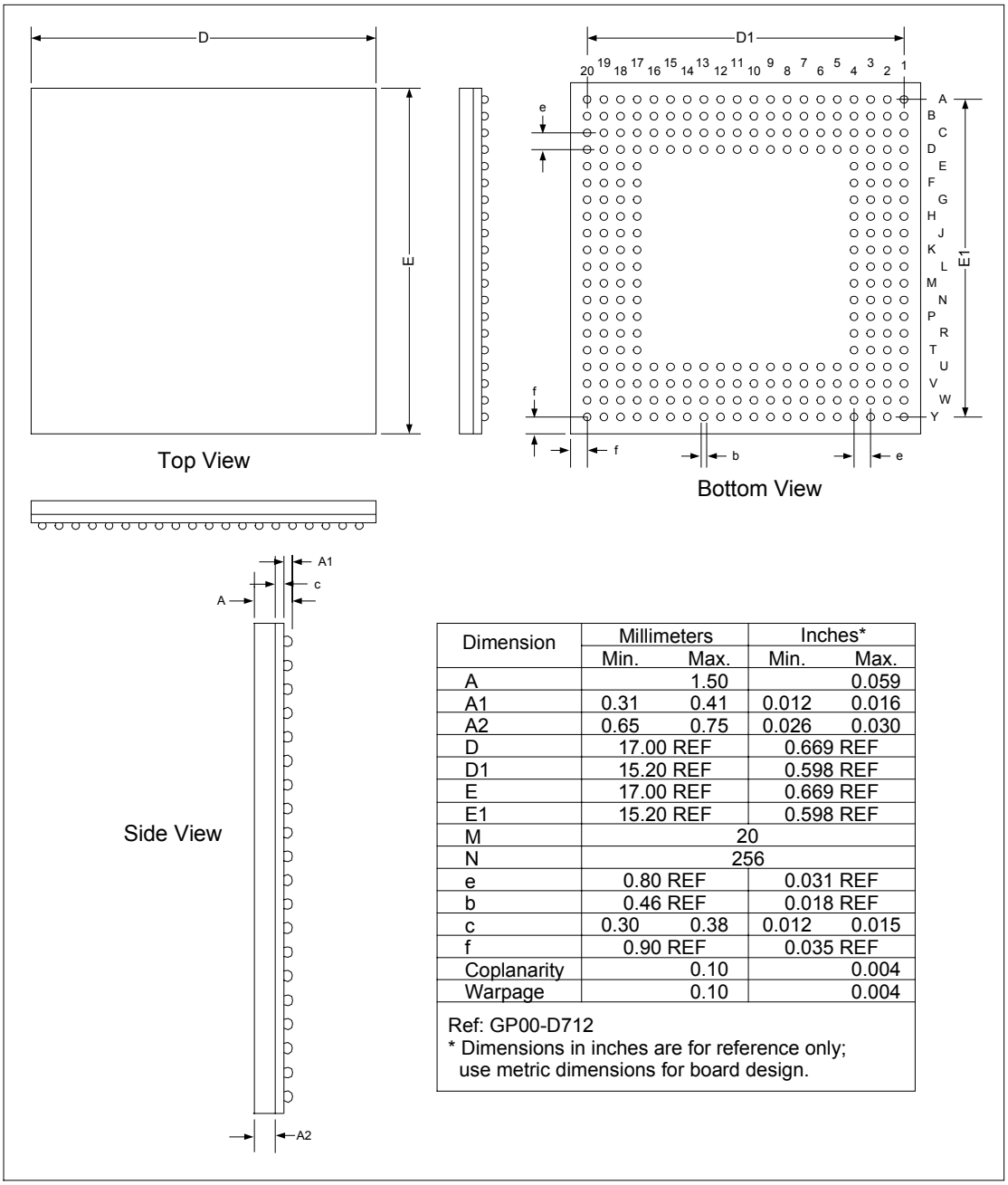
4 Package Dimensions

The package dimensions for the 17 mm x 17 mm FPBGA are shown in Figure 4-1.

Figure 4-1. Package Dimensions – 17 mm x 17 mm FPBGA



Dimension	Millimeters		Inches*	
	Min.	Max.	Min.	Max.
A		1.50		0.059
A1	0.31	0.41	0.012	0.016
A2	0.65	0.75	0.026	0.030
D	17.00 REF		0.669 REF	
D1	15.20 REF		0.598 REF	
E	17.00 REF		0.669 REF	
E1	15.20 REF		0.598 REF	
M	20			
N	256			
e	0.80 REF		0.031 REF	
b	0.46 REF		0.018 REF	
c	0.30	0.38	0.012	0.015
f	0.90 REF		0.035 REF	
Coplanarity		0.10		0.004
Warpage		0.10		0.004

Ref: GP00-D712
* Dimensions in inches are for reference only; use metric dimensions for board design.

PD_GP00-D712

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NOTES

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